ISSN: 0974-2115
www.jchps.com Journal of Chemical and Pharmaceutical Sciences

# Implementation of pass transistor logic in recursive parallel self-timed adder to achieve low power

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**ABSTRACT**

Parallel Self-timed adder is disclosed as (PASTA). The design is based on recursive formulation and half adders are used for executing multi-bit binary addition. The operation will be done parallel for the bits that doesn't need any carry chain propagation. In this approach the adder attains logarithmic performance when compared to other adders. In the existing design of PASTA only CMOS implementation is done. But in the proposed method Pass Transistor Logic implementation is done. The corresponding Pass Transistor Logic implementation of the design along with completion detection unit is presented. The main advantage of the proposed method is that power and the transistor count is decreased comprehensively when compared to that of the proposed method. The performance of the implementation is tested using Tanner circuit simulation tool. Simulation results show its superiority over other circuit adders and how efficient is the proposed method from other existing methods.

**KEY WORDS:** PASTA, Pass Transistor Logic, Fast adder, half adder

## 1. INTRODUCTION

One of the common arithmetic operation used in the circuits is addition. Based on this operation only the speed of the circuit is determined commonly. This operation becomes critical in DSP processors, floating point units, and ASIC processors. A delay or problem in this can entirely affect the performance of the circuits. In high speed addition generally there would be a trade-off between area and speed. In complex integrated circuits the binary adder play a major role. For improving the effectiveness and the operation of the circuit care must be taken on carry generation. For the improved performance the circuit must not wait for the arrival of carry. The carry must be driven to the output as soon as possible by this the path delay is reduced and consequently the performance gets improved. The optimization of the adders can be done in logic and circuit level. In logic level manipulation of equations and in circuit level the sizing of transistors and various circuit topologies can be done. Ultimately the optimization must not increase the circuit area.

**Theoretical Background:** The commonly used operation in all circuits is the binary addition. Generally the circuits are designed for synchronous clocking because it is simple and less time consuming. But this type of designing cannot be helpful for all the applications. Certain applications need clock less or the asynchronous circuits. The Asynchronous circuits does not dwell on time limitation. For these type of circuits the pipelined structure is commonly deployed. The above constraints for the asynchronous circuits add robustness to the circuit design and certainly have an effect in the operation. So for overcoming these shortcomings an effective and good alternate approach is needed, for that we are going for the Parallel Self Timed Adder (PASTA). The PASTA uses multiplexers and half adders for the operation. Here the main advantage is that the carry generation is recursive. So for the binary operation the two bits will be selected and based on the selected input the carry will be generated and stored. The Half adder feedback path ensures that the carry generation is recursive and does not terminate abruptly until the carry is generated for all the possible combinations. The generated carry is stored in the completion detection unit. The recursive loop will stop when all the carry results to zero.

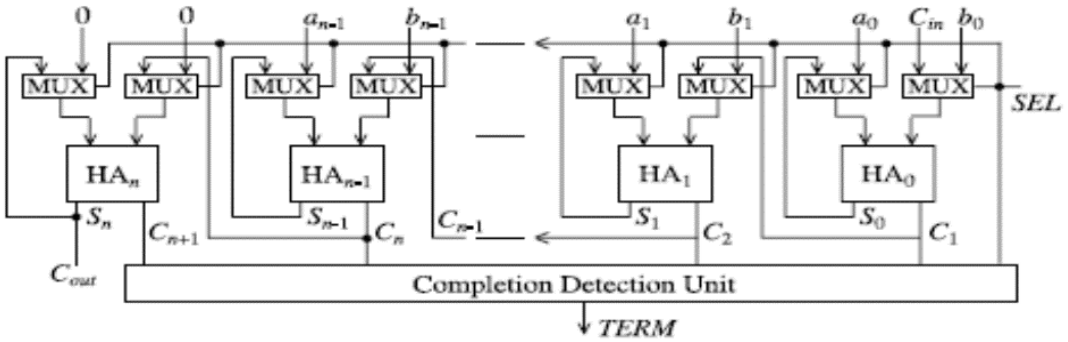


**Fig. 1. Exciting Parallel Self Timed Adder Configuration**

## 2. METHODS AND MATERIALS USED IN PROPOSED PASS TRANSISTOR LOGIC BASED SYSTEM

**Proposed System:** The normal CMOS implementation is good for circuits which are simple and easy to execute. For those circuits which have less switching there will be no problem but when a complex circuit with more number of switching and calculations is needed the existing method will not come handy. We are going for the

implementation of the PASS TRANSISTOR LOGIC when compared to other styles is that in this way of implementation the area and amount of power consumed is reduced comparatively. In the proposed method the Multiplexers and the Adder circuits are implemented using the Pass Transistor Logic, the completion detection unit will remain unchanged. While doing the required changes the total number of transistors required for each circuit is reduced to a considerable amount. When the total number of transistors are reduced automatically the size of the circuit gets reduced. When area gets reduced it indirectly supports for the reduction of the power consumption. But the main reason for the reduction in power is switching activity. With reduced switching activity and less number of gates the complexity is also reduced. In this implementation the main advantage will be realized when it is done with complex circuits which has more switching operations.

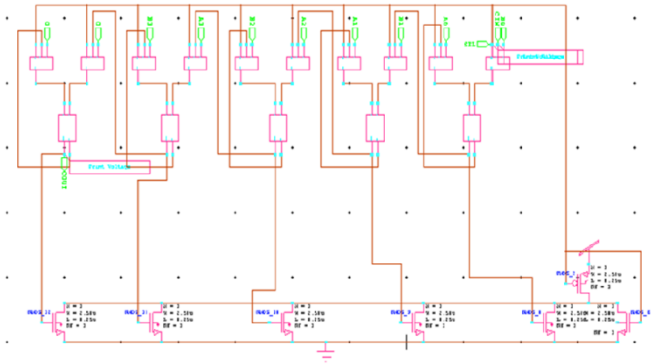

**Figure.2. Proposed system circuit diagram**

## 3. RESULT AND DISCUSSION

**Simulation of CMOS implementation:** In this graph the output for the various inputs of the PASTA is generated and this clearly shows how much the proposed method is lagging when compared to the proposed method

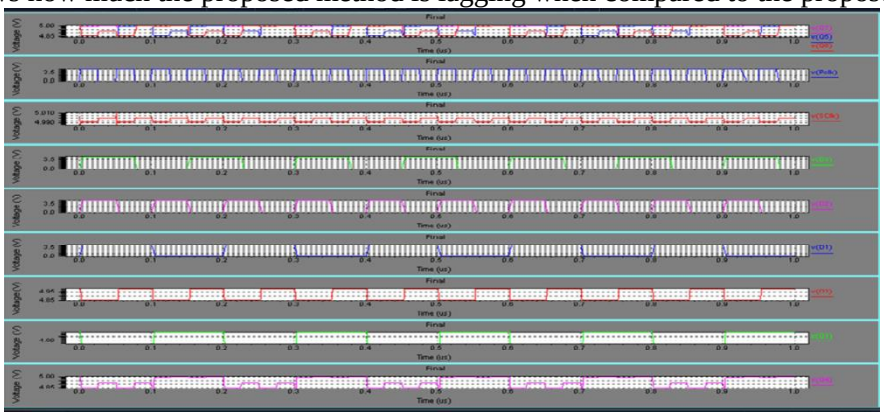

**Figure.3. Output for CMOS implementation of PASTA**

**Output for the Proposed Method:** In this graph the power consumption for the proposed method is depicted and it clearly indicates that the circuit is consuming less power than the existing system. The minimum power for the Pass transistor logic is 9.106289e-007 watts and the maximum power is 2.205275e-002 watts

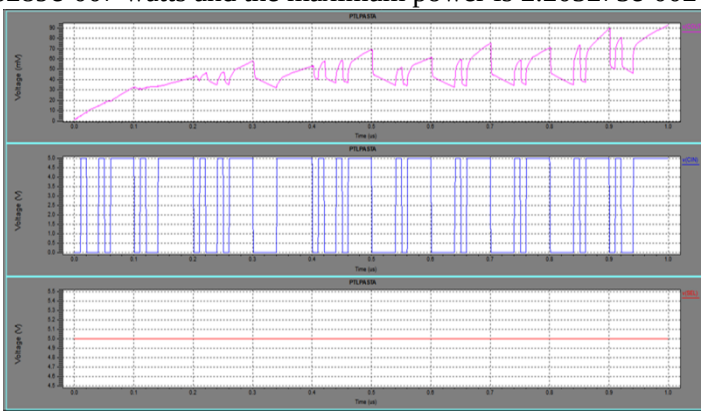

**Figure.4. Output for the Pass Transistor Logic Implementation**

**Output Comparison:**

**Table.1.Output Comparison**

| Pasta Logic | Minimum Power | Maximum Power | Average Power | Mosfet Count | Delay (ns) |
|---|---|---|---|---|---|
| CMOS | 1.078363e-008 watts | 1.590584e-001 watts | 9.263418e-004 watts | 197 | 6.9062e-008 |
| PassTransistor Logic | 9.106289e-007 watts | 2.205275e-002 watts | 1.402194e-002 watts | 57 | 1.0374e-008 |

While comparing the CMOS implementation and the proposed method the transistor count is reduced drastically and the power consumption is also reduced comprehensively. And the one of the major constraint for the binary operation is delay, and it is also reduced considerably. So the proposed method is more effective than the existing method.

## 4. CONCLUSION

In the proposed method the implementation of Parallel Self Timed Adder (PASTA) with the Pass Transistor Logic is done. This method is proposed to reduce the complexity and the time taken for the operation to complete. Adder circuits play a major role in the performance of the Digital Signal Processing, Multiplication and Accumulation unit, microprocessors and other applications. With this proposed work the performance of the circuit is improved considerably with less power consumed when compared to that of the normal CMOS implementation. We have concluded with simulation and comparison results of the existing Parallel Self Timed Adder and with the proposed work. The proposed method shows the circuit operates effectively while considering important performance parameters like power and delay. We designed and simulated our proposed circuit using Tanner EDA tool in 180nm technology

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